# Chapter1 Cevaxm4\_Subsystem

## Introduction

Cevaxm4\_Subsystem is a platform targeted for high-performance computer vision and image processing applications, which includes four CEVA-XM4 core. The CEVA-XM4 is an extremely powerful, low-power DSP processor designed and optimized for computer vision and image processing, which is based on a VLIW model combined with SIMD concept. This processor consists of 4 Scalar Processing Units (SPUs), two Load/Store Units (LSUs), a Program Control Unit (PCU), two Vector Processing Units (VPUs), a Power Scaling Unit (PSU), Memory Subsystem (MSS) and Emulation interface.

## Architecture



Figure 1 CevaXM4\_Subsystem Diagram

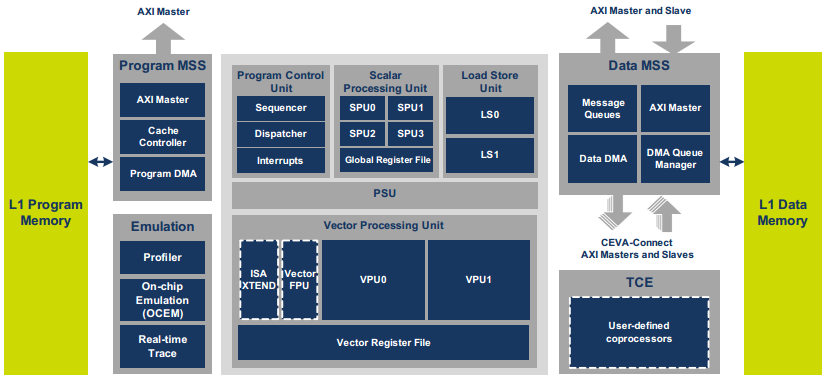


Figure 2 CEVA-XM4 DSP Block Diagram

## Features

1. The four CEVA-XM4 core can be power on/off respectively.
2. The four CEVA-XM4 core can communicate with each other in MCCI mode or interrupt mode.
3. High code compactness due to:

* Variable instruction width (16-bit, 32-bit, 48-bit and 64 bit)
* Variable-size instruction packets
* Instruction replication method

1. All instructions support predication:

* Conditional execution
* Reduces cycle count and code size on control and overhead code

1. Enhanced register file that also includes (every core)

* 32 32-bit general registers used for scalar operations and address generation
* 40 256-bit vector registers used for all vector-related operations

1. Every core includes two Vector Processing Units (VPUs):

* Parallel processing of up to 256-bits operations in each unit
* Supports 32 8-bit, 16 16-bit or 8 32-bit operations in each unit
* All operations are signed or unsigned
* Supports both inter-vector and intra-vector operations
* Up to 64 multipliers of 8x16 bits, 32 multipliers of 16x16 bits and 8 multipliers of 32x32 bits on each VPU
* Advanced filter operations for two-dimensional frames
* Up to 64 Sum of Absolute Differences (SADs) per cycle with an option to accumulate partial results
* Ability to sort vectors according to minimum, median and maximum
* Bit-manipulation operations including vector permutations
* Logical operations
* Non-linear operation support, such as , ,
* Supports up to 16 single-precision floating-point operations

1. Every core has Four Scalar Processing Units (SPUs):

* Supports 16-bit and 32-bit operations
* 16×16 bits, 32×16 bits and 32×32 bits multipliers
* 16×16 bits, 32×16 bits and 32×32 MAC operations
* Full support of bit-manipulation and logical unit
* Supports single-precision floating-point operations

1. Every core has Two Load/Store Units (LSUs) for two independent accesses to the data memories:
   * Maximum bandwidth of 512-bits when using both load units
   * Maximum bandwidth of 256-bits for store operations
   * Ability to access up to 32 different memory addresses in one memory access
   * Multiple data addressing modes, including:
   * Four gigabyte program and data address
   * Byte-addressable data address
   * Unaligned data memory access
2. Program memory subsystem that includes:
   * L1 program memory
   * L1 four-way program cache
   * Dedicated AXI master bus
   * Program Direct Memory Access (DMA) available for background transfers and cache preloading
3. Data memory subsystem that includes:

* L1 data memory
* Data DMA available for background data transfers
* DMA task queue manager
* Separate I/O space for peripherals’ connectivity

1. Fully registered memory interface
2. On-chip Emulation (OCEM) support via a JTAG port